

HX711 使用

ロードセル用 AD コンバータモジュール基板

AE-HX711-SIP

主な仕様

Arduino やマイコンなどに接続してロードセルの抵抗値の変化を測定し、重り等で校正をすることで、重さを量ることが出来ます。クロック (PD_SCK) とデータ (DOUT) の 2 信号で、Arduino などの GPIO で通信します。

弊社通販サイトに 参考用 Arduino サンプルスケッチがごさいます。GitHub に HX711 ライブラリがあり、ソフト制作の参考になります。ロードセルとは VDD・GND・INA+・INA- の 4 線で接続します。

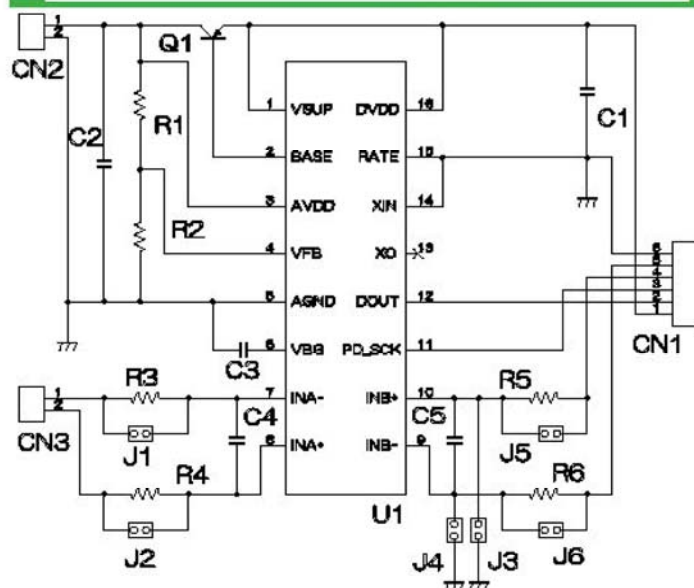
動作電圧 : 5V (4.5 ~ 5.5V)

出力データレート : 10sps

AD コンバータ分解能 : 24 ビット



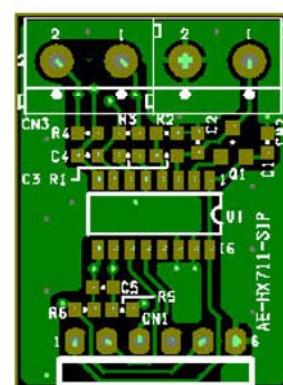
回路図



ピンアサイン

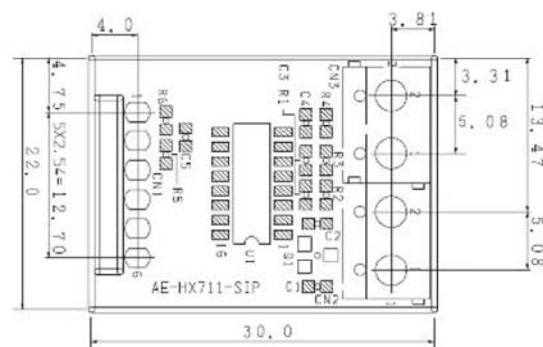
CN1	名称	機能
1	VDD	電源入力 DC5V
2	DAT	データ出力
3	CLK	クロック入力
4	INPB	Bch+ 入力
5	INNB	Bch- 入力
6	GND	GND
CN2	名称	機能
1	AVDD	ロードセル用電源
2	GND	GND
CN3	名称	機能
1	INNA	Ach- 入力
2	INPA	Ach+ 入力

CN3 CN2



CN1

基板外形



部品表

記号	値・定格	型番・備考
C1,C2	10uF 6.3V	
C3,4,5	0.1uF 50V	
Q1	トランジスタ	MMBT3906
R1	20k Ω	
R2	8.2k Ω	
R3 ~ R6	100 Ω	
U1	A/D コンバータ	HX711
CN1	ピンヘッダ 6P	
CN2,3	端子台	小型縦型 2 ピンタイプ

使用部品は変更となる場合が御座います。ご了承ください。

弊社通販サイトの本商品に関するページはこちらです。

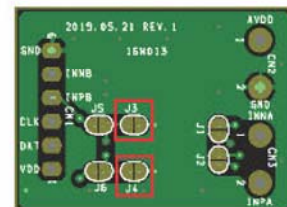
<http://akizukidenshi.com/catalog/g/gK-12370/>

株式会社 秋月電子通商

基板はんだジャンパー

・ J1、J2、J5、J6 は入力抵抗 100 Ω を「使用する」「使用しない」の選択です。通常は入力抵抗を使用しますので、はんだジャンパーしません。

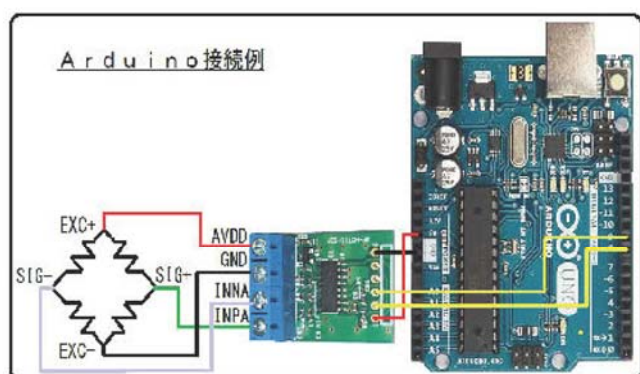
・ J3、J4 は B チャンネル入力を使用しない場合に GND に接続するはんだジャンパーです。通常は B チャンネル入力を使用しませんのではんだジャンパーしてください。



製作

- ・ CN1 はご用途に合わせて取り付け方向（上向き、下向き）をお選びください。
- ・ CN2、CN3 は側面の溝と突起をスライドさせて、2 個を組み合わせてからはんだ付けしてください。

Arduino 接続例



下記の表と接続例に従ってロードセルと CN2、3 の各ピンを、Arduino と CN1 の各ピンを接続します（商品ページ掲載のサンプルスケッチ用です）。

ロードセル	AE-HX711-SIP	Arduino
EXC+	AVDD	VDD
EXC-	GND	DAT
SIG-	INNA	CLK
SIG+	INPA	GND

参考資料

Pin #	Name	Function	Description
1	VSUP	Power	Regulator supply: 2.7 ~ 5.5V
2	BASE	Analog Output	Regulator control output (NC when not used)
3	AVDD	Power	Analog supply: 2.6 ~ 5.5V
4	VFB	Analog Input	Regulator control input (connect to AGND when not used)
5	AGND	Ground	Analog Ground
6	VBG	Analog Output	Reference bypass output
7	INA-	Analog Input	Channel A negative input
8	INA+	Analog Input	Channel A positive input
9	INB-	Analog Input	Channel B negative input
10	INB+	Analog Input	Channel B positive input
11	PD_SCK	Digital Input	Power down control (high active) and serial clock input
12	DOUT	Digital Output	Serial data output
13	XO	Digital I/O	Crystal I/O (NC when not used)
14	XI	Digital Input	Crystal I/O or external clock input, 0: use on-chip oscillator
15	RATE	Digital Input	Output data rate control, 0: 10Hz, 1: 80Hz
16	DVDD	Power	Digital supply: 2.6 ~ 5.5V

Table 1 Pin Description

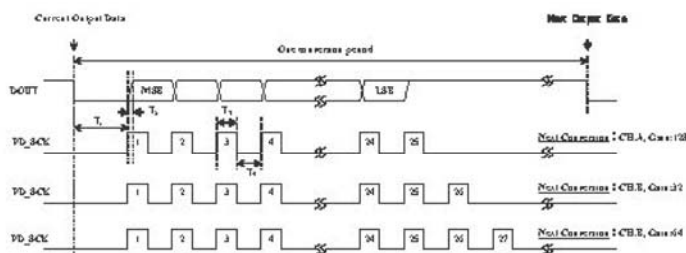


Fig.2 Data output, input and gain selection timing and control

KEY ELECTRICAL CHARACTERISTICS

Parameter	Notes	MIN	TYP	MAX	UNIT
Full scale differential input range	$V(\text{inp}) - V(\text{inn})$	$\pm 0.5(\text{AVDD}/\text{GAIN})$			V
Commonmode input		AGND+1.2		AVDD-1.3	V
Output data rate	Internal Oscillator, RATE = 0	10			Hz
	Internal Oscillator, RATE = DVDD	80			
Output data coding	Crystal or external clock, RATE = 0	$f_{\text{osc}}/1,105,920$			
	Crystal or external clock, RATE = DVDD	$f_{\text{osc}}/138,240$			
Output settling time ⁽¹⁾	RATE = 0	400			ms
	RATE = DVDD	50			
Input offset drift	Gain = 128	0.2			mV
	Gain = 64	0.4			
Input noise	Gain = 128, RATE = 0	50			nV(rms)
	Gain = 128, RATE = DVDD	90			
Temperature drift	Input offset (Gain = 128)	±6			nV/°C
	Gain (Gain = 128)	±5			ppm/°C
Input common mode rejection	Gain = 128, RATE = 0	100			dB
	Gain = 128, RATE = DVDD	100			
Power supply rejection	Gain = 128, RATE = 0	100			dB
	Gain = 128, RATE = DVDD	100			
Reference bypass (V _{FB})		12.5			V
Crystal or external clock frequency		1	11,059.2	20	MHz
Power supply voltage	DVDD	2.6		5.5	V
	AVDD, VSUP	2.6		5.5	
Analog supply current (including regulator)	Normal	1400			μA
	Power down	0.3			
Digital supply current	Normal	100			μA
	Power down	0.2			

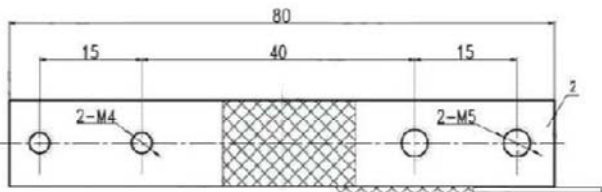
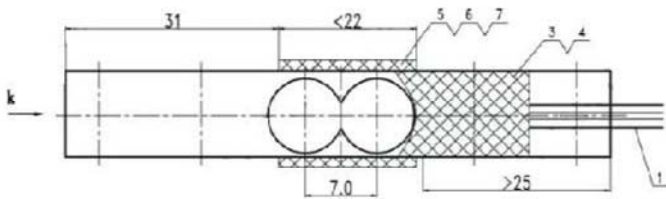
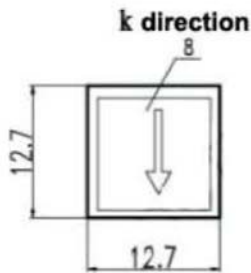
(1) Settling time refers to the time from power up, reset, input channel change and gain change to valid stable output data.

Table 2 Key Electrical Characteristics

詳細な資料は弊社通販サイトに掲載されています。



Size: 80x12.7x12.7 mm



SC133

Micro Type Load Cell

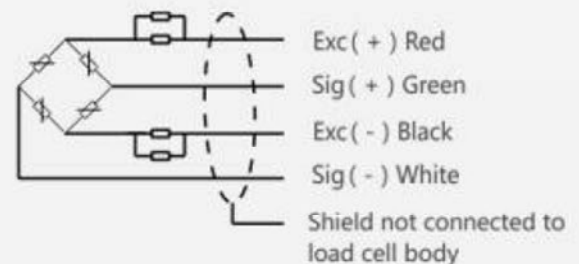


Apply to: Kitchen scale, vending machine, smart shelf, Robot, Coffee machine, dancing machine, Other force measuring device.

Specification:

Capacity	2kg
Rated output	1.0 ±0.15 mv/v
Accuracy	0.05 %F·S
Comprehensive Error	0.05 %F·S
Creep	±0.05 %F·S/3min
Non-linearity	±0.05 %F·S
hysteresis error	±0.05 %F·S
Repeatability	±0.05 %F·S
Zero output	±0.1mv/V
Temp. effect on sensitivity	0.05% F·S/10℃
Temp. effect on zero	0.2%F·S/10℃
Input resistance	1000 ± 10 Ω
Output resistance	1000 ±10 Ω
Insulation resistance	≥ 2000 MΩ
Temp. range	-10+40℃
Excitation voltage	3~10 VDC
Safe overload	150 %F·S
Four corner error	±0.1%F·S
Load cell material	Aluminum alloy
Connecting cable	Φ0.8x220mm
Unit weight	32 g/unit
Package	500 units / carton

Wiring:



24-Bit Analog-to-Digital Converter (ADC) for Weigh Scales

DESCRIPTION

Based on Avia Semiconductor's patented technology, HX711 is a precision 24-bit analog-to-digital converter (ADC) designed for weigh scales and industrial control applications to interface directly with a bridge sensor.

The input multiplexer selects either Channel A or B differential input to the low-noise programmable gain amplifier (PGA). Channel A can be programmed with a gain of 128 or 64, corresponding to a full-scale differential input voltage of $\pm 20\text{mV}$ or $\pm 40\text{mV}$ respectively, when a 5V supply is connected to AVDD analog power supply pin. Channel B has a fixed gain of 32. On-chip power supply regulator eliminates the need for an external supply regulator to provide analog power for the ADC and the sensor. Clock input is flexible. It can be from an external clock source, a crystal, or the on-chip oscillator that does not require any external component. On-chip power-on-reset circuitry simplifies digital interface initialization.

There is no programming needed for the internal registers. All controls to the HX711 are through the pins.

FEATURES

- Two selectable differential input channels
- On-chip active low noise PGA with selectable gain of 32, 64 and 128
- On-chip power supply regulator for load-cell and ADC analog power supply
- On-chip oscillator requiring no external component with optional external crystal
- On-chip power-on-reset
- Simple digital control and serial interface: pin-driven controls, no programming needed
- Selectable 10SPS or 80SPS output data rate
- Simultaneous 50 and 60Hz supply rejection
- Current consumption including on-chip analog power supply regulator:
 - normal operation $< 1.5\text{mA}$, power down $< 1\mu\text{A}$
- Operation supply voltage range: 2.6 ~ 5.5V
- Operation temperature range: $-40 \sim +85^{\circ}\text{C}$
- 16 pin SOP-16 package

APPLICATIONS

- Weigh Scales
- Industrial Process Control

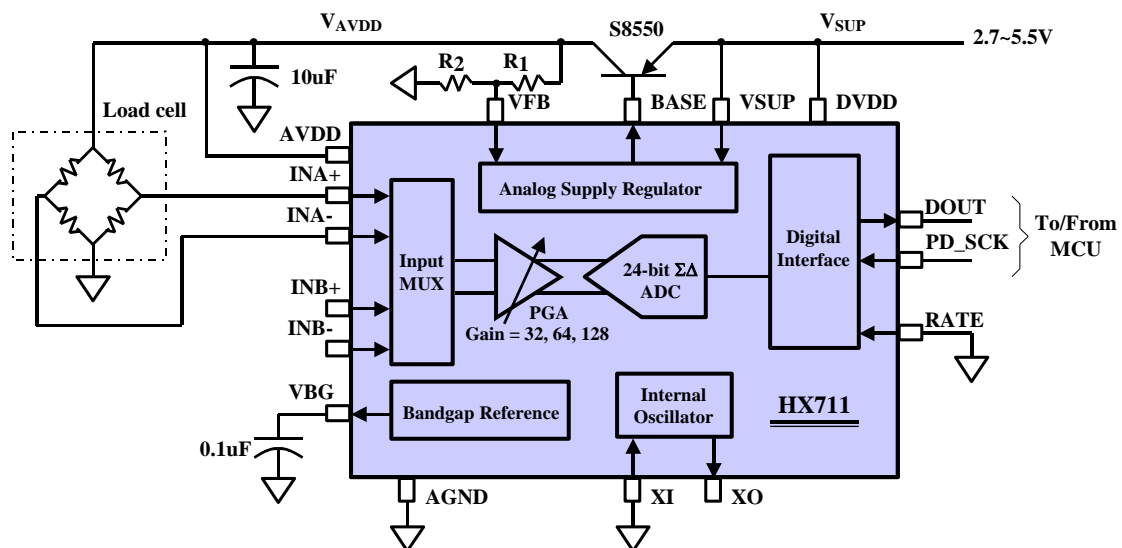
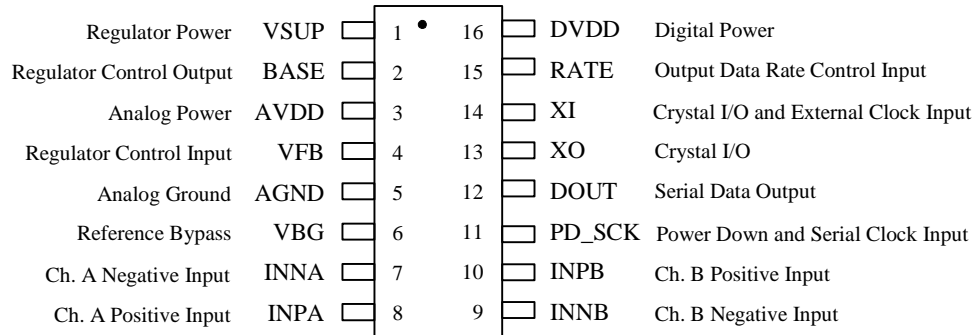


Fig. 1 Typical weigh scale application block diagram

Pin Description


SOP-16L Package

Pin #	Name	Function	Description
1	VSUP	Power	Regulator supply: 2.7 ~ 5.5V
2	BASE	Analog Output	Regulator control output (NC when not used)
3	AVDD	Power	Analog supply: 2.6 ~ 5.5V
4	VFB	Analog Input	Regulator control input (connect to AGND when not used)
5	AGND	Ground	Analog Ground
6	VBG	Analog Output	Reference bypass output
7	INA-	Analog Input	Channel A negative input
8	INA+	Analog Input	Channel A positive input
9	INB-	Analog Input	Channel B negative input
10	INB+	Analog Input	Channel B positive input
11	PD_SCK	Digital Input	Power down control (high active) and serial clock input
12	DOUT	Digital Output	Serial data output
13	XO	Digital I/O	Crystal I/O (NC when not used)
14	XI	Digital Input	Crystal I/O or external clock input, 0: use on-chip oscillator
15	RATE	Digital Input	Output data rate control, 0: 10Hz; 1: 80Hz
16	DVDD	Power	Digital supply: 2.6 ~ 5.5V

Table 1 Pin Description

KEY ELECTRICAL CHARACTERISTICS

Parameter	Notes	MIN	TYP	MAX	UNIT
Full scale differential input range	V(inp)-V(inn)	$\pm 0.5(AVDD/GAIN)$			V
Common mode input		AGND+1.2		AVDD-1.3	V
Output data rate	Internal Oscillator, RATE = 0		10		Hz
	Internal Oscillator, RATE = DVDD		80		
	Crystal or external clock, RATE = 0		$f_{clk}/1,105,920$		
	Crystal or external clock, RATE = DVDD		$f_{clk}/138,240$		
Output data coding	2's complement	800000		7FFFFFF	HEX
Output settling time ⁽¹⁾	RATE = 0		400		ms
	RATE = DVDD		50		
Input offset drift	Gain = 128		0.2		mV
	Gain = 64		0.4		
Input noise	Gain = 128, RATE = 0		50		nV(rms)
	Gain = 128, RATE = DVDD		90		
Temperature drift	Input offset (Gain = 128)		± 6		nV/°C
	Gain (Gain = 128)		± 5		ppm/°C
Input common mode rejection	Gain = 128, RATE = 0		100		dB
Power supply rejection	Gain = 128, RATE = 0		100		dB
Reference bypass (V _{BG})			1.25		V
Crystal or external clock frequency		1	11.0592	20	MHz
Power supply voltage	DVDD	2.6		5.5	V
	AVDD, VSUP	2.6		5.5	
Analog supply current (including regulator)	Normal		1400		μA
	Power down		0.3		
Digital supply current	Normal		100		μA
	Power down		0.2		

(1) Settling time refers to the time from power up, reset, input channel change and gain change to valid stable output data.

Table 2 Key Electrical Characteristics

Analog Inputs

Channel A differential input is designed to interface directly with a bridge sensor's differential output. It can be programmed with a gain of 128 or 64. The large gains are needed to accommodate the small output signal from the sensor. When 5V supply is used at the AVDD pin, these gains correspond to a full-scale differential input voltage of $\pm 20\text{mV}$ or $\pm 40\text{mV}$ respectively.

Channel B differential input has a fixed gain of 32. The full-scale input voltage range is $\pm 80\text{mV}$, when 5V supply is used at the AVDD pin.

Power Supply Options

Digital power supply (DVDD) should be the same power supply as the MCU power supply.

When using internal analog supply regulator, the dropout voltage of the regulator depends on the external transistor used. The output voltage is equal to $V_{AVDD} = V_{BG} * (R1 + R2) / R2$ (Fig. 1). This voltage should be designed with a minimum of 100mV below VSUP voltage.

If the on-chip analog supply regulator is not used, the VSUP pin should be connected to either AVDD or DVDD, depending on which voltage is higher. Pin VFB should be connected to Ground and pin BASE becomes NC. The external 0.1uF bypass capacitor shown on Fig. 1 at the VBG output pin is then not needed.

Clock Source Options

By connecting pin XI to Ground, the on-chip oscillator is activated. The nominal output data rate when using the internal oscillator is 10 (RATE=0) or 80SPS (RATE=1).

If accurate output data rate is needed, crystal or external reference clock can be used. A crystal can be directly connected across XI and XO pins. An external clock can be connected to XI pin, through a 20pF ac coupled capacitor. This external clock is not required to be a square wave. It can come directly from the crystal output pin of the MCU chip, with amplitude as low as 150 mV.

When using a crystal or an external clock, the internal oscillator is automatically powered down.

Output Data Rate and Format

When using the on-chip oscillator, output data rate is typically 10 (RATE=0) or 80SPS (RATE=1).

When using external clock or crystal, output data rate is directly proportional to the clock or crystal frequency. Using 11.0592MHz clock or crystal results in an accurate 10 (RATE=0) or 80SPS (RATE=1) output data rate.

The output 24 bits of data is in 2's complement format. When input differential signal goes out of the 24-bit range, the output data will be saturated at 800000h (MIN) or 7FFFFFFh (MAX), until the input signal comes back to the input range.

Serial Interface

Pin PD_SCK and DOUT are used for data retrieval, input selection, gain selection and power down controls.

When output data is not ready for retrieval, digital output pin DOUT is high. Serial clock input PD_SCK should be low. When DOUT goes to low, it indicates data is ready for retrieval. By applying 25~27 positive clock pulses at the PD_SCK pin, data is shifted out from the DOUT output pin. Each PD_SCK pulse shifts out one bit, starting with the MSB bit first, until all 24 bits are shifted out. The 25th pulse at PD_SCK input will pull DOUT pin back to high (Fig.2).

Input and gain selection is controlled by the number of the input PD_SCK pulses (Table 3). PD_SCK clock pulses should not be less than 25 or more than 27 within one conversion period, to avoid causing serial communication error.

PD_SCK Pulses	Input channel	Gain
25	A	128
26	B	32
27	A	64

Table 3 Input Channel and Gain Selection

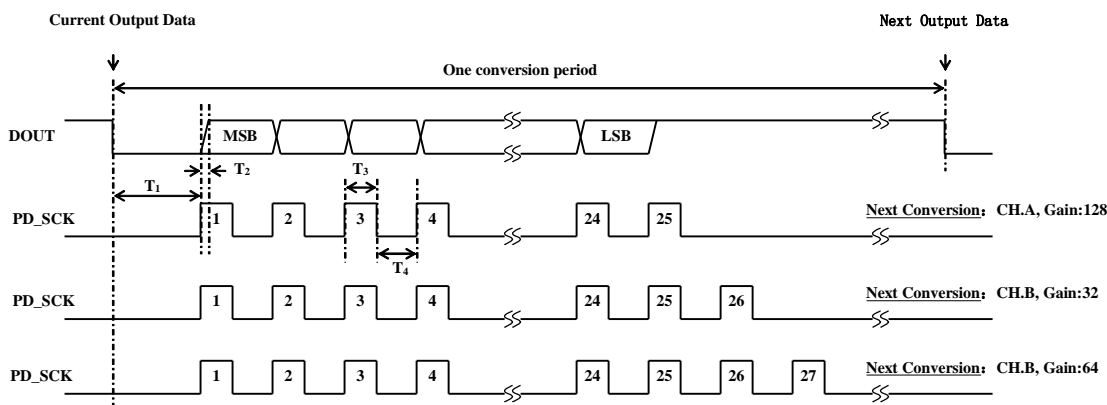


Fig.2 Data output, input and gain selection timing and control

Symbol	Note	MIN	TYP	MAX	Unit
T ₁	DOUT falling edge to PD_SCK rising edge	0.1			□ μs
T ₂	PD_SCK rising edge to DOUT data ready			0.1	□ μs
T ₃	PD_SCK high time	0.2	1	50	□ μs
T ₄	PD_SCK low time	0.2	1		□ μs

Reset and Power-Down

When chip is powered up, on-chip power on rest circuitry will reset the chip.

Pin PD_SCK input is used to power down the HX711. When PD_SCK Input is low, chip is in normal working mode.

powered down. When PD_SCK returns to low, chip will reset and enter normal operation mode.

After a reset or power-down event, input selection is default to Channel A with a gain of 128.

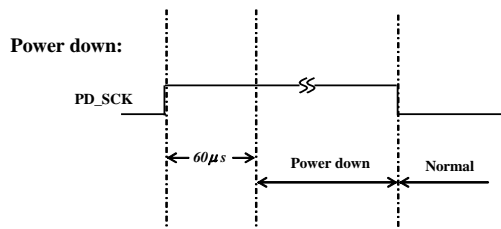


Fig.3 Power down control

When PD_SCK pin changes from low to high and stays at high for longer than 60μs, HX711 enters power down mode (Fig.3). When internal regulator is used for HX711 and the external transducer, both HX711 and the transducer will be

Application Example

Fig.1 is a typical weigh scale application using HX711. It uses on-chip oscillator (XI=0), 10Hz output data rate (RATE=0). A Single power supply (2.7~5.5V) comes directly from MCU power supply. Channel B can be used for battery level detection. The related circuitry is not shown on Fig. 1.

Reference PCB Board (Single Layer)

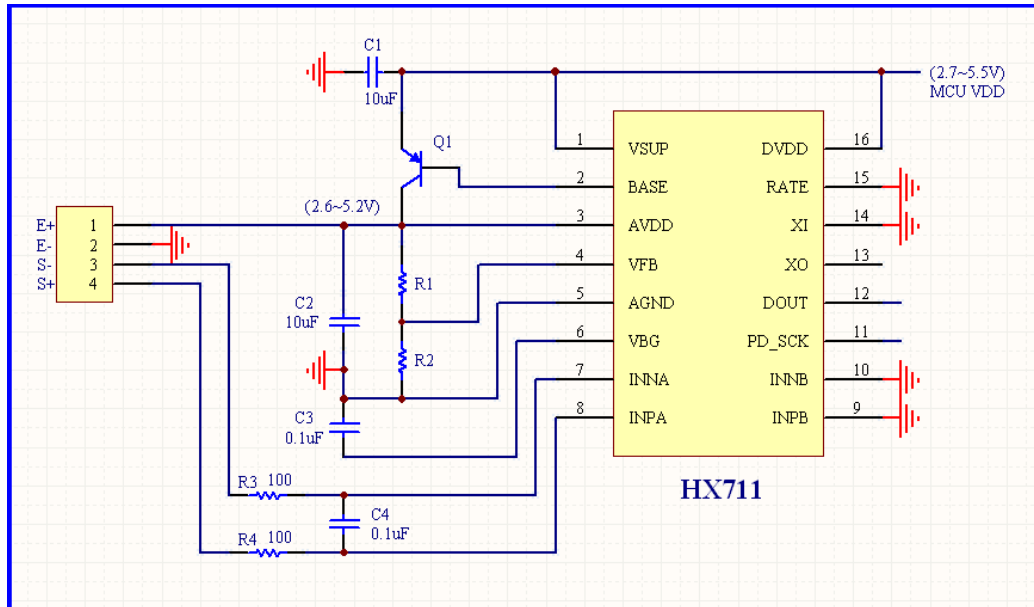


Fig.4 Reference PCB board schematic

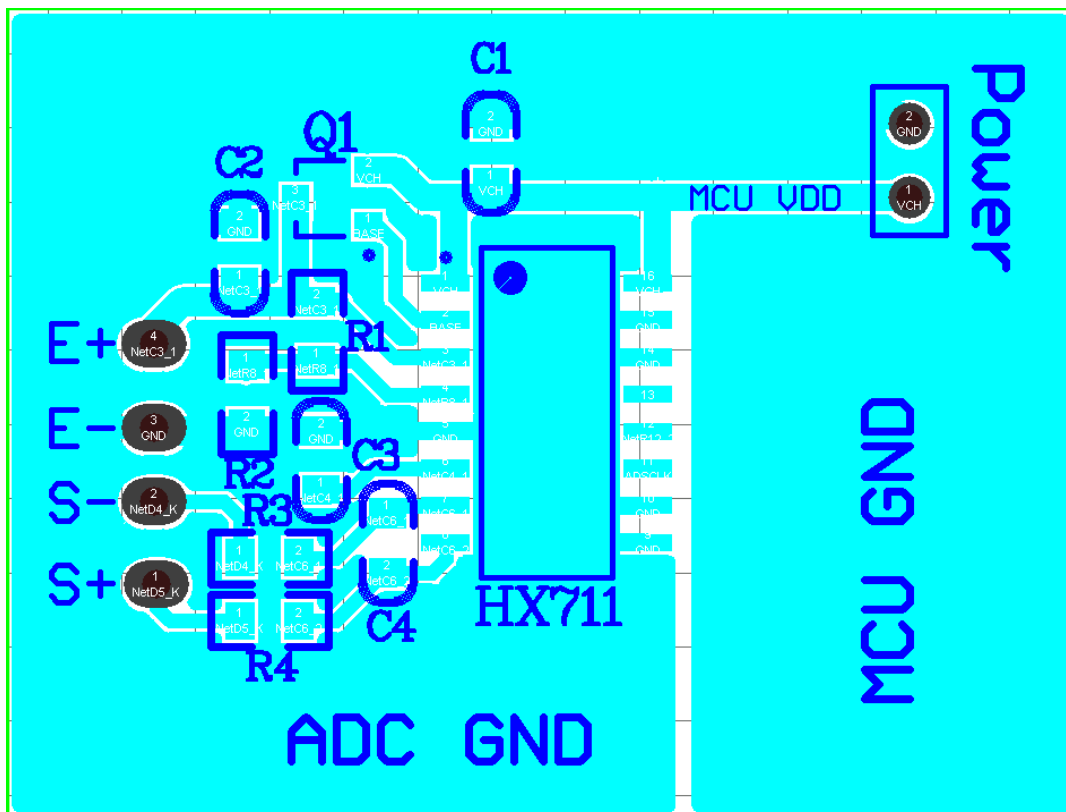


Fig.5 Reference PCB board layout

Reference Driver (Assembly)

```

/*-----*/
Call from ASM:      LCALL   ReaAD
Call from C:       extern unsigned long ReadAD(void);
                   .
                   .
                   unsigned long data;
                   data=ReadAD();
                   .
                   .
-----*/

PUBLIC      ReadAD
HX711ROM    segment code
rseg       HX711ROM

sbit       ADDO = P1.5;
sbit       ADSK = P0.0;
/*-----*/
OUT:   R4, R5, R6, R7   R7=>LSB
-----*/

ReadAD:
    CLR   ADSK           //AD Enable (PD_SCK set low)
    SETB  ADDO           //Enable 51CPU I/O
    JB    ADDO,$         //AD conversion completed?
    MOV   R4,#24

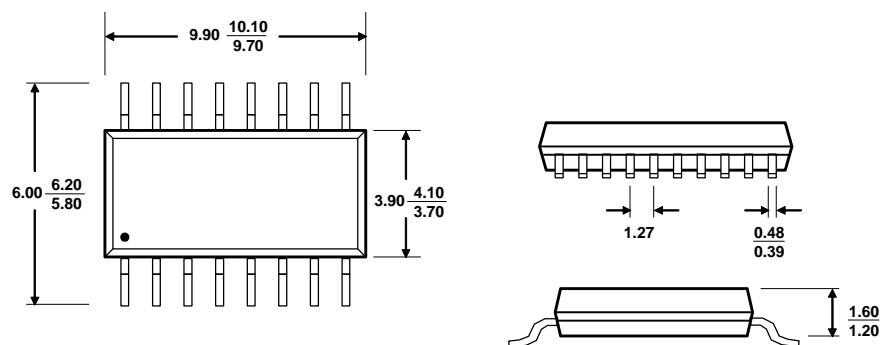
ShiftOut:
    SETB  ADSK           //PD_SCK set high (positive pulse)
    NOP
    CLR   ADSK           //PD_SCK set low
    MOV   C,ADD0         //read on bit
    XCH  A,R7           //move data
    RLC  A
    XCH  A,R7
    XCH  A,R6
    RLC  A
    XCH  A,R6
    XCH  A,R5
    RLC  A
    XCH  A,R5
    DJNZ  R4,ShiftOut   //moved 24BIT?
    SETB  ADSK
    NOP
    CLR   ADSK
    RET
    END

```

Reference Driver (C)

```
//-----
sbit  ADD0 = P1^5;
sbit  ADSK = P0^0;
unsigned long ReadCount(void) {
    unsigned long Count;
    unsigned char i;
    ADD0=1;
    ADSK=0;
    Count=0;
    while(ADD0);
    for (i=0;i<24;i++){
        ADSK=1;
        Count=Count<<1;
        ADSK=0;
        if(ADD0) Count++;
    }
    ADSK=1;
    Count=Count^0x800000;
    ADSK=0;
    return(Count);
}
```

Package Dimensions



Typ MAX
 MIN Unit: mm

SOP-16L Package